

What is claimed is:

1 1. A baud-rate timing recovery system for recovering timing information from a transmitted
2 signal, the system comprising:

3 a sampler having first and second inputs and an output, the first input adapted to receive
4 a transmitted signal, the second input adapted to receive a clock signal, the sampler operative to
5 sample a transmitted signal according to the clock signal;

6 a DFE having an input and first and second outputs, the input coupled to the output of
7 the sampler, the DFE having a first pre-cursor tap providing the first output and a first post-
8 cursor tap providing the second output; and

9 a timing error detector having first and second inputs and an output, the first input
10 coupled to the first output of the DFE and the second input coupled to the second output of the
11 DFE, the timing error detector operative to provide at the output a signal representative of the
12 timing error reflected in the sampled transmitted signal, the signal provided at the output of the
13 timing error detector being used to derive the clock signal at the second input of the sampler.

1 2. The baud-rate timing recovery system of claim 1, wherein the system further comprises:

2 a loop filter having an input and an output, the input coupled to the output of the timing
3 error detector, the loop filter operative to filter the signal provided by the timing error detector;
4 and

5 a VCO having an input and an output, the input coupled to the output of the loop filter,
6 the output coupled to the second input of the sampler, the VCO operative to provide a clock
7 signal as a function of the voltage supplied by the loop filter.

1 3. The baud-rate timing recovery system of claim 1, wherein the system further comprises:

2 a NCO having an input and an output, the input of the NCO coupled to the output of the

3 timing error detector, the output of the NCO coupled to the second input of the sampler, the NCO
4 operative to provide a clock signal as a function of the signal supplied by the timing error
5 detector.

1 4. The baud-rate timing recovery system of claim 1, wherein the timing error detector
2 comprises

3 timing function means for providing at the output a signal representative of the timing
4 error reflected in the sampled transmitted signal, the timing function means operative to provide
5 a signal that is the weighted sum of the first pre-cursor and the first post-cursor.

1 5. The baud-rate timing recovery system of claim 1, wherein the DFE has a third output, the
2 DFE having a main tap for providing the third output and wherein the timing error detector has a
3 third input, the third input coupled to the third output of the DFE.

1 6. The baud-rate timing recovery system of claim 1, wherein the timing error detector
2 comprises

3 timing function means for providing at the output a signal representative of the timing
4 error reflected in the sampled transmitted signal, the timing function means operative to provide
5 a signal according to the timing function: $z_0(n) = \alpha_0 \frac{b(1)}{w(N-1)} + \beta_0 \frac{w(N-2)}{w(N-1)^2}$.

1 7. The baud-rate timing recovery system of claim 1, wherein the timing error detector
2 comprises

3 timing function means for providing at the output a signal representative of the timing
4 error reflected in the sampled transmitted signal, the timing function means operative to provide
5 a signal according to the timing function: $z_1(n) = \alpha_1 b(1) + \beta_1 \frac{w(N-2)}{w(N-1)}$.

1 8. The baud-rate timing recovery system of claim 1, wherein the timing error detector
2 comprises

3 timing function means for providing at the output a signal representative of the timing
4 error reflected in the sampled transmitted signal, the timing function means operative to provide
5 a signal according to the timing function: $z_2(n) = \alpha_2 b(1)w(N - 1) + \beta_2 w(N - 2)$.

1 9. A baud-rate timing recovery method for recovering timing information from a transmitted
2 signal, the method comprising:

3 sampling a transmitted signal using a sampler having first and second inputs and an
4 output, the first input adapted to receive a transmitted signal, the second input adapted to receive
5 a clock signal, the sampler operative to sample a transmitted signal according to the clock signal;

6 equalizing the sampled, transmitted signal using a DFE having an input and first and
7 second outputs, the input coupled to the output of the sampler, the DFE having a first pre-cursor
8 tap providing the first output and a first post-cursor tap providing the second output; and

9 deriving a signal representative of a timing error reflected in the sampled, transmitted
10 signal using a timing error detector having first and second inputs and an output, the first input
11 coupled to the first output of the DFE and the second input coupled to the second output of the
12 DFE, the timing error detector operative to provide the signal representative of the timing error at
13 the output, the signal provided at the output of the timing error detector being used to derive the
14 clock signal at the second input of the sampler.

1 10. The baud-rate timing recovery method of claim 9, wherein deriving a signal representative
2 of a timing error comprises:

3 using a timing error detector having timing function means for providing at the output a
4 signal representative of the timing error, the timing function means operative to provide a signal

5 that is the weighted sum of the first pre-cursor and the first post-cursor.

1 11. The baud-rate timing recovery method of claim 9, wherein equalizing the sampled,
2 transmitted signal comprises using a DFE having a third output, the DFE having a main tap for
3 providing the third output; and

4 wherein deriving a signal representative of a timing error comprises using a timing error
5 detector having a third input, the third input coupled to the third output of the DFE.

1 12. The baud-rate timing recovery method of claim 9, wherein deriving a signal representative
2 of a timing error comprises:

3 using a timing error detector having timing function means for providing at the output a
4 signal representative of the timing error, the timing function means operative to provide a signal
5 according to the timing function: $z_0(n) = \alpha_0 \frac{b(1)}{w(N-1)} + \beta_0 \frac{w(N-2)}{w(N-1)^2}$.

1 13. The baud-rate timing recovery method of claim 9, wherein deriving a signal representative
2 of a timing error comprises:

3 using a timing error detector having timing function means for providing at the output a
4 signal representative of the timing error, the timing function means operative to provide a signal
5 according to the timing function: $z_1(n) = \alpha_1 b(1) + \beta_1 \frac{w(N-2)}{w(N-1)}$.

1 14. The baud-rate timing recovery method of claim 9, wherein deriving a signal representative
2 of a timing error comprises:

3 using a timing error detector having timing function means for providing at the output a
4 signal representative of the timing error, the timing function means operative to provide a signal
5 according to the timing function: $z_2(n) = \alpha_2 b(1)w(N-1) + \beta_2 w(N-2)$.

1 15. A baud-rate timing recovery system for recovering timing information from a transmitted
2 signal, the system comprising:

3 an ADC having first and second inputs and an output, the first input adapted to receive a
4 transmitted signal, the second input adapted to receive a clock signal, the ADC operative to
5 sample a transmitted signal according to the clock signal;

6 a DFE operative to equalize a transmitted signal, the DFE comprising:

7 a FFF having an input and at least first, second, and third outputs, the input
8 coupled to the output of the sampler, the FFF having at least a first pre-cursor tap providing the
9 first output and a main tap providing the second output, the FFF operative to reduce at least one
10 precursor in the sampled transmitted signal to produce a forward filtered signal on the third
11 output;

12 subtraction logic having first and second inputs and an output, the first input
13 coupled to the third output of the FFF, the subtraction logic operative to subtract the signal on the
14 second input from the signal on the first input;

15 decision logic having an input and an output, the input coupled to the output of
16 the subtraction logic, the decision logic operative to decide on a state of a sampled symbol; and

17 a FBF having a first input and first and second outputs, the input coupled to the
18 output of the decision logic, the FBF having at least a first post-cursor tap providing the first
19 output, the FBF operative to reduce post-cursors in the sampled transmitted signal to produce a
20 feedback filtered signal at the second output, the second output coupled to the second input of
21 the subtraction logic; and

22 a timing error detector having first, second, and third inputs and an output, the first input
23 coupled to the first output of the FBF, the second input coupled to the second output of the FFF,
24 and the third input coupled to the first output of the FFF, the timing error detector operative to

25 provide at the output a signal representative of the timing error reflected in the sampled
26 transmitted signal, the signal provided at the output of the timing error detector being used to
27 derive the clock signal at the second input of the ADC.

1 16. The baud-rate timing recovery system of claim 15, wherein the system further comprises:
2 a loop filter having an input and an output, the input coupled to the output of the timing
3 error detector, the loop filter operative to filter the signal provided by the timing error detector;
4 and
5 a VCO having an input and an output, the input coupled to the output of the loop filter,
6 the output coupled to the second input of the ADC, the VCO operative to provide a clock signal
7 as a function of the voltage supplied by the loop filter.

1 17. The baud-rate timing recovery system of claim 15, wherein the system further comprises:
2 a NCO having an input and an output, the input of the NCO coupled to the output of the
3 timing error detector, the output of the NCO coupled to the second input of the ADC, the NCO
4 operative to provide a clock signal as a function of the signal supplied by the timing error
5 detector.

1 18. The baud-rate timing recovery system of claim 15, wherein the timing error detector
2 comprises
3 timing function means for providing at the output a signal representative of the timing
4 error reflected in the sampled transmitted signal, the timing function means operative to provide
5 a signal according to the timing function: $z_0(n) = \alpha_0 \frac{b(1)}{w(N-1)} + \beta_0 \frac{w(N-2)}{w(N-1)^2}$.

1 19. The baud-rate timing recovery system of claim 15, wherein the timing error detector
2 comprises

3 timing function means for providing at the output a signal representative of the timing
4 error reflected in the sampled transmitted signal, the timing function means operative to provide
5 a signal according to the timing function: $z_1(n) = \alpha_1 b(1) + \beta_1 \frac{w(N-2)}{w(N-1)}$.

1 20. The baud-rate timing recovery system of claim 15, wherein the timing error detector
2 comprises

3 timing function means for providing at the output a signal representative of the timing
4 error reflected in the sampled transmitted signal, the timing function means operative to provide
5 a signal according to the timing function: $z_2(n) = \alpha_2 b(1)w(N-1) + \beta_2 w(N-2)$.